Ref: dPMR MoU tech.lib-Test Modes-v1

Source: dPMR MoU

Title: Tests Modes Supported by dPMR Equipment.

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Introduction

dPMR terminals compliant with the protocols in TS 102 490 (Tier I) and TS 102 658 (Tier II) require RF conformance testing to EN 301 166-2. This document details dPMR MoU recommended test modes that manufacturers may support to simplify connectivity between equipment and test systems.

dPMR Test Functions

dPMR Pseudo-Random Data Test Pattern (dPRd)

The dPMR Pseudo-Random data test pattern (dPRd) is a preamble followed by a Frame Sync followed by repeating PN sequences as follows:

Where:

P: Preamble, minimum of 72 bits as defined in TS 102 490
FS1: 48 bit Frame Sync 1 sequence as defined in TS 102 490
PN: 511 bit PN sequence as defined in EN 301 166

Further information is given in the annexes of this document, however the ETSI specifications referenced above should be considered the normative sources.

dPMR Receiver Test Interface

A test typical test configuration for a dPMR receiver section is shown in Figure 1. It is assumed that the signal generator will generated the dPMR Pseudo-Random data test pattern (dPRd), as defined in section 0.
The receiver should be placed in a test mode where it receives the test signal as a valid dPMR transmission and supplies the received data at a suitable interface connector.

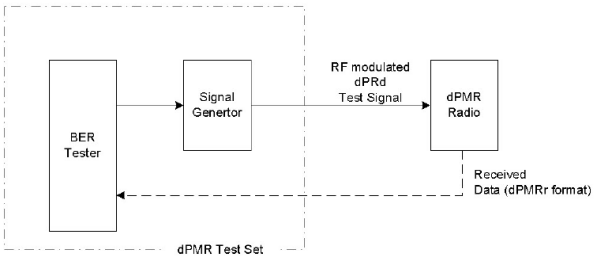
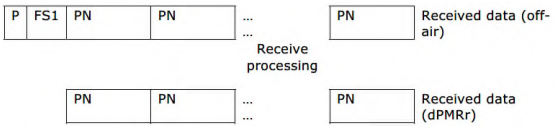


Figure 1 – Typical dPMR BER test configuration

The output format shall be the dPMR received data interface (dPMRr) which is the received data with the pre-amble and FS1 omitted (shown diagrammatically in below:



dPMRr received data format

dPMRr Signal Format

The signal shall be NRZ data at 4800 bps.

dPMRr Electrical Levels

The signals shall be LVTTL (3V) meeting the following conditions:
V_{OH} = 2.0 V at I_{OH} = -20 mA V_{OL} = 0.55 V at I_{OL} = 32mA

Alternative Interfaces

Clock and Gate

The equipment may provide a clock associated with the data. Where a clock is provided it should have a duty cycle of better than 30% / 70% and have a rising edge nominally centred on the associated data bit.

If provided, the clock should only be active while received data is present unless either a clock gating signal or a trigger signal is provided. A clock gating signal should be active high when received data is present. A trigger signal shall be high during the first bit of received data.

RS232

The dPMRr data may be presented as RS232 data on a suitable output port. If this mode is used the RS232 should be configured as:

Bit rate: 9600 Data bits: 8 Parity bits: 0 Stop bits: 1 (9600, 8,n,1)

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Annex A (informative) – TS 102 490 definitions

Preamble

The preamble consists of a minimum of 72 bits and shall have the form 5F 5F 5F 5F 5F 5F 5F 5F 5F.

If a preamble pattern longer than 72 bits is used then the repeated 5F pattern (01011111) shall be maintained.
This represents a series of modulation systems +3,+3,-3,-3,+3,+3,-3,-3 etc.

Frame Sync (FS1)

The Frame sync 1 sequence is a 48 bit sequence that shall have the following value:

Binary:
010101111111111101011111011101011101010101110111.

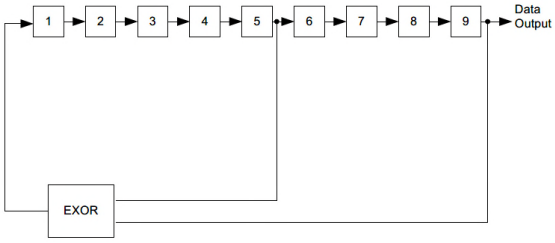
Hex: 57 FF 5F 75 D5 77.

Annex B (informative) – EN 301 166 definitions

PN Sequence
The pseudo-random bit sequence shall be of at least 511 bits (as defined in ITU-T Recommendation O.153), at 4800 bits/sec.

The PN generator hardware is shown below. The shift register shall be initiated with 111111111, i.e. the first 9 bits in the sequence shall be 1.

511 bit 9-bit PRBS generator



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